WHAT IS CLAIMED IS:

1. An apparatus for inserting a DFD (design-for-debug) circuitry in an integrated circuit to debug or diagnose scan cores each having a selected fault type and a scan clock; said apparatus comprising:

(a) a DFD selector for indicating which said scan cores and said selected fault types will be debugged or diagnosed simultaneously;

(b) a scan connector for connecting multiple scan chains in said scan cores to a boundary-scan chain in said integrated circuit;

(c) a scan clock generator for generating an ordered sequence of capture clocks for connection to said scan clocks in said scan cores; and

(d) a multiplexer for connecting said DFD selector and said scan connector to a TAP (test access port) controller in said integrated circuit.

2. The apparatus of claim 1, further comprising a scan debug mode; wherein said scan debug mode is set to logic value 1 when said scan cores are to be diagnosed, and set to logic value 0 when said scan cores are not to be diagnosed.

3. The apparatus of claim 2, wherein said scan debug mode is generated by a central DFD controller; wherein said DFD controller interfaces with said TAP controller and said DFD circuitry; and wherein said TAP controller is constructed according to a selected Boundary-scan Standard which includes a test access port (TAP) comprising TDI (test data in), TDO (test data out), TCK (test clock), TMS (test mode select), and selectively TRSTB (test reset).

4. The apparatus of claim 1, wherein said selected fault types further comprise stuck-type faults and non-stuck-type delay faults; wherein said stuck-type faults include stuck-at faults, bridging faults, and IDDQ (IDD quiescent current) faults; and wherein said non-stuck-type delay faults include transition (gate-delay) faults, path-delay faults, memory read/write faults, and multiple-cycle delay faults.

5. The apparatus of claim 3, wherein said DFD selector further comprises using a shift register of 2 or more bits in each said scan core to indicate whether said scan core will be diagnosed and what said selected fault type shall be targeted; wherein said shift register is controlled by said TCK and its scan data input and scan data output are connected to said TDI and said TDO via said multiplexer, respectively.

6. The apparatus of claim 3, wherein said scan connector further comprises using a plurality of multiplexers to stitch said multiple scan chains together as one serial scan chain and connect its scan data input and scan data output to said TDI and said TDO, respectively; wherein said multiplexers are controlled by said scan debug mode.

7. The apparatus of claim 3, wherein said scan connector further comprises using a plurality of multiplexers to stitch said multiple scan chains together as one serial scan chain and insert said serial scan chain before or after said boundary-scan chain; wherein said multiplexers are controlled by said scan debug mode.

8. The apparatus of claim 3, wherein said scan connector further comprises using a plurality of

multiplexers to stitch only those scan cells within all said multiple scan chains which share the same said scan clock together as one single scan chain, called grouped scan chain; wherein said grouped scan chain connects its scan data input and scan data output to said TDI and said TDO, respectively; and wherein said multiplexers are controlled by said scan debug mode.

9. The apparatus of claim 1, wherein said scan connector further comprises selectively inserting an inverter and a lock-up element between any two said multiple scan chains when stitched together to form a serial scan chain or a grouped scan chain; wherein said lock-up element is a selected D latch or D flip-flop.

10. The apparatus of claim 3, wherein said scan clock generator for generating an ordered sequence of capture clocks further comprises a clock phase generator and a scan clock controller.

11. The apparatus of claim 10, wherein said clock phase generator is controlled by said TCK and generates a plurality of non-overlapping TCK clocks; and wherein said scan clock controller is controlled by said selected fault type and connects said capture clocks, comprising said TCK, said non-overlapping TCK clocks, and non-overlapping system clocks, to said scan clocks in said scan cores; wherein said non-overlapping system clocks are generated by the system clocks external to said integrated circuit or on an ATE (automatic test equipment).

12. The apparatus of claim 11, wherein said non-overlapping TCK clocks are used to debug or diagnose said stuck-type faults, including said stuck-at faults, said

bridging faults, and said IDDQ faults, in said scan cores in said integrated circuit.

13. The apparatus of claim 11, wherein said non-overlapping system clocks are used to debug or diagnose said non-stuck-type delay faults, including said transition (gate-delay) faults, said path-delay faults, said memory read/write faults, and said multiple-cycle delay faults, in said scan cores in said integrated circuit.

14. The apparatus of claim 11, wherein said scan clock controller further comprises a generator for generating a global scan enable (GSE) signal to control the shift and capture operations of said multiple scan chains in said scan cores; wherein said generator for generating a global scan enable (GSE) signal is further generated by said TAP controller, including Shift_DR, Capture_DR, and Update_DR, according to said selected Boundary-scan Standard.

15. The apparatus of claim 1, wherein said DFD circuitry is further selected for debugging or diagnosing memory scan cores.

16. An apparatus for inserting a DFD (design-for-debug) circuitry in an integrated circuit to debug or diagnose memory BIST (built-in self-test) cores each having a selected fault type and a MBIST (memory BIST) clock; said apparatus comprising:

(a) a DFD selector for indicating which said memory BIST cores and said selected fault types will be debugged or diagnosed simultaneously;

(b) a MBIST debug register in each said memory BIST core for storing selected data of said memory BIST core during diagnosis;

(c) a skip register in each said memory BIST core for storing a predetermined number of MBIST clock cycles or errors to be skipped in one said memory BIST core during diagnosis;

(d) a MBIST debug controller in each said memory BIST core for controlling the memory BIST operation of the memory BIST controller in said memory BIST core; and

(e) a multiplexer for connecting said DFD selector, said MBIST debug registers, and said skip registers, to a TAP (test access port) controller in said integrated circuit.

17. The apparatus of claim 16, further comprising a MBIST debug mode; wherein said MBIST debug mode is set to logic value 1 when said memory BIST cores are to be diagnosed, and set to logic value 0 when said memory BIST cores are not to be diagnosed.

18. The apparatus of claim 17, wherein said MBIST debug mode is generated by a central DFD controller; wherein said DFD controller interfaces with said TAP controller and said DFD circuitry; and wherein said TAP controller is constructed according to a selected Boundary-scan Standard which includes a test access port (TAP) comprising TDI (test data in), TDO (test data out), TCK (test clock), TMS (test mode select), and selectively TRSTB (test reset).

19. The apparatus of claim 16, wherein said selected fault types further include memory read/write faults and data retention faults.

20. The apparatus of claim 18, wherein said DFD selector further comprises using a shift register of 2 or more bits in each said memory BIST core to indicate whether

said memory BIST core will be diagnosed and what said selected fault type shall be targeted; wherein said shift register is controlled by said TCK and its scan data input and scan data output are connected to said TDI and said TDO via said multiplexer, respectively.

21. The apparatus of claim 18, wherein said MBIST debug register stores said selected data comprising selected MBIST finish signal, memory address, error memory index, output data, error signal, status codes, and other selected registers and signals in one said memory BIST core.

22. The apparatus of claim 21, wherein all said MBIST debug registers are stitched together as a first shift register to shift said selected data out to said TDO via said multiplexer for diagnosis; wherein said first shift register is controlled by said TCK; and said multiplexer is controlled by said MBIST debug mode.

23. The apparatus of claim 18, wherein all said skip registers are stitched together as a second shift register to shift said predetermined number of MBIST clock cycles or errors in through TDI and out through said TDO via said multiplexer for diagnosis; wherein said second shift register is controlled by said TCK; and said multiplexer is controlled by said MBIST debug mode.

24. The apparatus of claim 16, wherein said MBIST debug controller further comprises:

(a) means for setting a BIST mode to logic value 1 (or 0) and signaling said memory BIST controller embedded in said memory BIST core to start (or stop) said memory BIST operation;

(b) means for setting an error signal to logic value 1 and halting said memory BIST operation of said memory BIST controller immediately whenever a memory BIST error is detected and said predetermined number of MBIST clock cycles or errors is reached; wherein said means are controlled by said memory BIST controller embedded in said memory BIST core; and said memory BIST controller is controlled by said MBIST clock;

(c) means for capturing said selected data of said memory BIST core to said MBIST debug register and shifting said selected data out of said MBIST debug register periodically using a diagnosis scan enable signal controlled by said TAP controller, including Shift_DR; and

(d) means for signaling said memory BIST controller to continue said memory BIST operation and reset said error signal to logic value 0 during or after shifting said selected data of said MBIST debug register out for diagnosis using a continue signal controlled by said TAP controller, including Update_DR.

25. The apparatus of claim 16, wherein said DFD circuitry is further selected for debugging or diagnosing PLL (phase-locked loop) BIST cores, DAC (digital-to-analog converter) BIST cores, ADC (analog-to-digital converter) BIST cores, and other BIST cores generating error signals.

26. An apparatus for inserting a DFD (design-for-debug) circuitry in an integrated circuit to debug or diagnose logic BIST (built-in self-test) cores each having a selected fault type and a LBIST (logic BIST) clock; said apparatus comprising:

(a) a DFD selector for indicating which said logic BIST cores and said selected fault types will be debugged or diagnosed simultaneously;

(b) a seed register in each said logic BIST core for storing selected data of said logic BIST core during diagnosis;

(c) a scan connector for connecting multiple scan chains in said logic BIST cores to a boundary-scan chain in said integrated circuit;

(d) a LBIST debug controller for controlling the logic BIST operation of the logic BIST controller in each said logic BIST core; and

(e) a multiplexer for connecting said DFD selector and said scan connector to a TAP (test access port) controller in said integrated circuit.

27. The apparatus of claim 26, further comprising a LBIST debug mode; wherein said LBIST debug mode is set to logic value 1 when said logic BIST cores are to be diagnosed, and set to logic value 0 when said logic BIST cores are not to be diagnosed.

28. The apparatus of claim 27, wherein said LBIST debug mode is generated by a central DFD controller; wherein said DFD controller interfaces with said TAP controller and said DFD circuitry; and wherein said TAP controller is constructed according to a selected Boundary-scan Standard which includes a test access port (TAP) comprising TDI (test data in), TDO (test data out), TCK (test clock), TMS (test mode select), and selectively TRSTB (test reset).

29. The apparatus of claim 26, wherein said selected fault types further comprise stuck-type faults and non-stuck-type delay faults; wherein said stuck-type faults include stuck-at faults, bridging faults, and IDDQ (IDD quiescent current) faults; and wherein said non-stuck-type

delay faults include transition (gate-delay) faults, path-delay faults, and multiple-cycle delay faults.

30. The apparatus of claim 28, wherein said DFD selector further comprises using a shift register of 2 or more bits in each said logic BIST core to indicate whether said logic BIST core will be diagnosed and what said selected fault type shall be targeted; wherein said shift register is controlled by said TCK and its scan data input and scan data output are connected to said TDI and said TDO via said multiplexer, respectively.

31. The apparatus of claim 28, wherein said seed register stores said selected data comprising selected LBIST finish signal, pseudorandom pattern generator (PRPG) outputs, cycle counter outputs, multiple-input signature register (MISR) outputs, cycle-end signal, scan-chain mask, cycle-mask start index, cycle-mask stop index, and other selected registers and signals in said logic BIST core; and further said seed register is selectively constructed by using a separate LBIST debug register or by reconfiguring the existing registers and signals storing said selected data as a shift register.

32. The apparatus of claim 31, wherein said LBIST debug register is controlled by said TCK; and wherein said shift register is controlled by said TCK during the shift operation and by said LBIST clock during said logic BIST operation; said seed registers comprising either said LBIST debug registers or said shift registers are further stitched together as a chip-level shift register with its scan data input and scan data output connected to said TDI and said TDO, respectively.

33. The apparatus of claim 28, wherein said scan connector further comprises using a plurality of multiplexers to stitch said multiple scan chains together as one serial scan chain and connect its scan data input and scan data output to said TDI and said TDO, respectively; wherein said multiplexers are controlled by said LBIST debug mode.

34. The apparatus of claim 28, wherein said scan connector further comprises using a plurality of multiplexers to stitch said multiple scan chains together as one serial scan chain and insert said serial scan chain before or after said boundary-scan chain; wherein said multiplexers are controlled by said LBIST debug mode.

35. The apparatus of claim 28, wherein said scan connector further comprises using a plurality of multiplexers to stitch only those scan cells within all said multiple scan chains which share the same said scan clock together as one single scan chain, called grouped scan chain; wherein said grouped scan chain connects its scan data input and scan data output to said TDI and said TDO, respectively; and wherein said multiplexers are controlled by said LBIST debug mode.

36. The apparatus of claim 26, wherein said scan connector further comprises selectively inserting an inverter and a lock-up element between any two said multiple scan chains when stitched together to form a serial scan chain or a grouped scan chain; wherein said lock-up element is a selected D latch or D flip-flop.

37. The apparatus of claim 26, wherein said scan connector for connecting multiple scan chains in said logic BIST cores to the boundary-scan chain in said integrated

circuit further comprises means for connecting said seed registers to said boundary-scan chain.

38. The apparatus of claim 26, wherein said LBIST debug controller further comprises:

(a) means for setting a BIST mode to logic value 1 (or 0) and signaling said logic BIST controller embedded in said logic BIST core to start (or stop) said logic BIST operation;

(b) means for setting a cycle-end signal to logic value 1 and halting said logic BIST operation of said logic BIST controller immediately whenever said logic BIST controller embedded in said logic BIST core has run through a predetermined number of LBIST clock cycles; wherein said means are controlled by said logic BIST controller embedded in said logic BIST core; and said logic BIST controller is controlled by said LBIST clock;

(c) means for capturing said selected data of said logic BIST core into said seed register and shifting a new seed into and said selected data out of said seed register periodically using a diagnosis scan enable signal controlled by said TAP controller, including Shift_DR; and

(d) means for signaling said logic BIST controller to continue said logic BIST operation and reset said cycle-end signal to logic value 0 during or after shifting said seed in and shifting selected data of said seed register out for diagnosis using a continue signal controlled by said TAP controller, including Update_DR.

39. The apparatus of claim 26, wherein said DFD circuitry is further selected for debugging or diagnosing other BIST cores generating cycle-end signals, including ROM (read-only memory) BIST cores.

40. An apparatus for inserting a DFD (design-for-debug) circuitry in an integrated circuit to debug or diagnose functional cores each having a selected fault type and a system clock; said apparatus comprising:

(a) a DFD selector for indicating which said functional cores and said selected fault types will be debugged or diagnosed simultaneously;

(b) a plurality of break registers in each said functional core which are stitched together for storing predetermined break conditions during diagnosis;

(c) a step counter in each said functional core for storing a predetermined number of clock cycles during diagnosis;

(d) a scan connector for connecting multiple scan chains in said functional cores to a boundary-scan chain in said integrated circuit;

(e) a RESET control circuitry that resets the contents of said functional cores when a reset control signal is set to logic value 1;

(f) a BREAK control circuitry in a functional clock controller that accepts a break condition signal from a said functional core to stop said system clock immediately when a break control signal is set to logic value 1 and a said predetermined break condition is met;

(g) a RUN control circuitry in said functional clock controller that allows said system clocks to run forever when a run control signal is set to logic value 1;

(h) a STEP control circuitry in said functional clock controller that accepts a step limit signal from a said functional core to stop said system clock immediately when a step control signal is set to logic value 1 and said system clock has run for an additional, said predetermined number of clock cycles.

(i) a STOP control circuitry in said functional clock controller that stops said system clocks when a stop control signal is set to logic value 1; and

(j) a multiplexer for connecting said DFD selector and said scan connector to a TAP (test access port) controller in said integrated circuit.

41. The apparatus of claim 40, further comprising a functional debug mode; wherein said functional debug mode is set to logic value 1 when said functional cores are to be diagnosed, and set to logic value 0 when said functional cores are not to be diagnosed.

42. The apparatus of claim 41, wherein said functional debug mode is generated by a central DFD controller; wherein said DFD controller interfaces with said TAP controller and said DFD circuitry; and wherein said TAP controller is constructed according to a selected Boundary-scan Standard which includes a test access port (TAP) comprising TDI (test data in), TDO (test data out), TCK (test clock), TMS (test mode select), and selectively TRSTB (test reset).

43. The apparatus of claim 40, wherein said selected fault types further comprise stuck-type faults and non-stuck-type delay faults; wherein said stuck-type faults include stuck-at faults, bridging faults, and IDDQ (IDD quiescent current) faults; and wherein said non-stuck-type delay faults include transition (gate-delay) faults, path-delay faults, memory read/write faults, and multiple-cycle delay faults.

44. The apparatus of claim 42, wherein said DFD selector further comprises using a shift register of 2 or more bits in each said functional core to indicate whether

said functional core will be diagnosed and what said selected fault type shall be targeted; wherein said shift register is controlled by said TCK and its scan data input and scan data output are connected to said TDI and said TDO via said multiplexer, respectively.

45. The apparatus of claim 42, wherein said break control circuitry further comprises means for shifting in said predetermined break conditions using said TCK to said break registers in said functional cores via said TDI.

46. The apparatus of claim 42, wherein said step control circuitry further comprises means for shifting in said predetermined number of clock cycles using said TCK to said step counters in said functional cores via said TDI.

47. The apparatus of claim 42, wherein said scan connector further comprises using a plurality of multiplexers to stitch said multiple scan chains together as one serial scan chain and connect its scan data input and scan data output to said TDI and said TDO, respectively; wherein said multiplexers are controlled by said functional debug mode.

48. The apparatus of claim 42, wherein said scan connector further comprises using a plurality of multiplexers to stitch said multiple scan chains together as one serial scan chain and insert said serial scan chain before or after said boundary-scan chain; wherein said multiplexers are controlled by said functional debug mode.

49. The apparatus of claim 42, wherein said scan connector further comprises using a plurality of multiplexers to stitch only those scan cells within all said multiple scan chains which share the same said scan

clock together as one single scan chain, called grouped scan chain; wherein said grouped scan chain connects its scan data input and scan data output to said TDI and said TDO, respectively; and wherein said multiplexers are controlled by said functional debug mode.

50. The apparatus of claim 40, wherein said scan connector further comprises selectively inserting an inverter and a lock-up element between any two said multiple scan chains when stitched together to form a serial scan chain or a grouped scan chain; wherein said lock-up element is a selected D latch or D flip-flop.

51. The apparatus of claim 40, wherein said scan connector for connecting multiple scan chains in said functional cores to a boundary-scan chain in said integrated circuit further comprises means for connecting said break registers and said step counters to said boundary-scan chain.

52. A method for debugging or diagnosing a plurality of scan cores, each having a selected fault type and a scan clock, with an embedded DFD (design-for-debug) circuitry in an integrated circuit; said method comprising the steps of:

(a) issuing a DBG_SCAN command for generating a scan debug mode to control said DFD circuitry in said scan cores;

(b) issuing a SELECT command for shifting in selected scan cores and said selected fault types to be debugged or diagnosed to the DFD selector of said DFD circuitry in said scan cores;

(c) issuing a first SHIFT command or a first plurality of SHIFT_CHAIN commands for shifting in a predetermined scan pattern to all scan cells within selected scan chains in said scan cores for diagnosis;

(d) issuing one or more CAPTURE commands for capturing output responses into all said scan cells in said scan cores;

(e) issuing a second SHIFT command or a second plurality of SHIFT_CHAIN commands for shifting a new predetermined scan pattern into and output response out of all said scan cells within said selected scan chains in said scan cores for diagnosis;

(f) repeating steps of (d)-(e) until scan diagnosis is done; and

(g) issuing a STOP command for generating a stop control signal to stop the scan operation.

53. The method of claim 52, further comprising providing a central DFD controller for accepting said commands and generating said scan debug mode and said stop control signal to control said DFD circuitry; wherein said DFD controller interfaces with said DFD circuitry and a TAP (test access port) controller in said integrated circuit; and wherein said TAP controller is constructed according to a selected Boundary-scan Standard.

54. The method of claim 52, wherein said selected fault type is used to detect or locate single or multiple errors arising from stuck-type faults or non-stuck-type delay faults in a said selected scan core; wherein said stuck-type faults include stuck-at faults, bridging faults, and IDDQ faults; and wherein said non-stuck-type delay faults include transition (gate-delay) faults, path-delay faults, memory read/write faults, and multiple-cycle delay faults.

55. The method of claim 52, wherein said commands are further used to debug or diagnose memory scan cores.

56. A method for debugging or diagnosing a plurality of memory BIST (built-in self-test) cores, each having a selected fault type and a MBIST (memory BIST) clock, with an embedded DFD (design-for-debug) circuitry in an integrated circuit; said method comprising the steps of:

(a) issuing a DBG_MBIST command for generating a MBIST debug mode to control said DFD circuitry in said memory BIST cores;

(b) issuing a SELECT command for shifting in selected memory BIST cores and said selected fault types to be debugged or diagnosed to the DFD selector of said DFD circuitry in said memory BIST cores;

(c) issuing a SKIP command for signaling the memory BIST controller in selected said memory BIST core to skip a predetermined number of MBIST clock cycles or errors;

(d) issuing a RUN command for generating a run control signal to continue the memory BIST operation of said memory BIST controller in each said memory BIST core whenever a new error is found and said predetermined number of MBIST clock cycles or errors are reached;

(e) issuing a CAPTURE command for capturing selected data in said memory BIST cores into a plurality of MBIST debug registers in said DFD circuitries over a predetermined sampling period;

(f) issuing a SHIFT command for shifting out said selected data in said MBIST debug registers for diagnosis;

(g) repeating step (d) and steps of (e)-(f) concurrently until memory BIST diagnosis is done; and

(h) issuing a STOP command for generating a stop control signal to stop said memory BIST operation.

57. The method of claim 56, further comprising providing a central DFD controller for accepting said commands and generating said MBIST debug mode and said control signals to control said DFD circuitry; wherein said

DFD controller interfaces with said DFD circuitry and a TAP (test access port) controller in said integrated circuit; and wherein said TAP controller is constructed according to a selected Boundary-scan Standard.

58. The method of claim 56, wherein each said selected fault type is used to detect or locate single or multiple memory BIST errors arising from faults including memory read/write faults or data retention faults in said selected memory BIST core.

59. The method of claim 56, wherein said commands are further used to debug or diagnose other BIST cores generating error signals, including PLL (phase-locked loop) BIST cores, DAC (digital-to-analog) BIST cores, and ADC (analog-to-digital) BIST cores.

60. A method for debugging or diagnosing a plurality of logic BIST (built-in self-test) cores, each having a selected fault type and a LBIST (logic BIST) clock, with an embedded DFD (design-for-debug) circuitry in an integrated circuit; said method comprising the steps of:

(a) issuing a DBG_LBIST command for generating a LBIST debug mode to control said DFD circuitry in said logic BIST cores;

(b) issuing a SELECT command for shifting in selected logic BIST cores and said selected fault types to be debugged or diagnosed to the DFD selector of said DFD circuitry in said logic BIST cores;

(c) issuing a first SHIFT command for shifting in predetermined starting seeds, each comprising a predetermined number of LBIST clock cycles, to a plurality of seed registers in said logic BIST cores;

(d) issuing a RUN command for generating a run control signal to continue the logic BIST operation of the

logic BIST controller in each said selected logic BIST core until said predetermined number of LBIST clock cycles stored in said logic BIST controller is reached;

(e) issuing a second SHIFT command for selectively shifting in expected responses of said seed registers for on-chip comparison or shifting out output responses of said seed registers for off-chip comparison over a predetermined sampling period;

(f) issuing a third SHIFT command for shifting in selected new seeds, each comprising a new predetermined number of LBIST clock cycles, to said seed registers;

(g) repeating steps of (d)-(f) until logic BIST diagnosis is done; and

(h) issuing a STOP command for generating a stop control signal to stop said logic BIST operation.

61. The method of claim 60, further comprising providing a central DFD controller for accepting said commands and generating said LBIST debug mode and said control signals to control said DFD circuitry; wherein said DFD controller interfaces with said DFD circuitry and a TAP (test access port) controller in said integrated circuit; and wherein said TAP controller is constructed according to a selected Boundary-scan Standard.

62. The method of claim 60, wherein said selected fault type is used to detect or locate single or multiple signature errors arising from stuck-type faults or non-stuck-type delay faults in a said selected logic BIST core; wherein said stuck-type faults include stuck-at faults, bridging faults, and IDDQ (IDD quiescent current) faults; and wherein said non-stuck-type delay faults include transition (gate-delay) faults, path-delay faults, memory read/write faults, and multiple-cycle delay faults.

63. The method of claim 60, wherein said step (e) further comprises comparing said output responses against said expected responses on-chip or off-chip; wherein each said output response or each said expected response includes the signature of the MISR (multiple-input signature register) in each said selected logic BIST core.

64. The method of claim 60, wherein said step (f) further comprises picking said new seed using a selected linear search or binary search method to locate said single or multiple signature errors in said MISR in each said selected logic BIST core.

65. The method of claim 60, wherein said commands are further used to debug or diagnose other BIST cores generating cycle-end signals, including ROM (read-only memory) BIST cores.

66. A method for debugging or diagnosing a plurality of functional cores, each having a selected fault type and a system clock, with an embedded DFD (design-for-debug) circuitry in an integrated circuit; said method comprising:

(a) issuing a DBG_FUNCTION command for generating a functional debug mode to control said DFD circuitry in said functional cores;

(b) issuing a SELECT command for shifting in selected functional cores and said selected fault types to be debugged or diagnosed to the DFD selector of said DFD circuitry in said functional cores;

(c) issuing a RESET command for generating a reset control signal to control said DFD circuitry in said functional cores;

(d) issuing one or more BREAK commands for shifting in predetermined break conditions to stop said system clocks in said functional cores;

(e) issuing a RUN command for generating a run control signal to control said DFD circuitry in said functional cores;

(f) issuing a first SHIFT command or a first plurality of SHIFT_CHAIN commands for shifting data into and out of all said scan cells within selected scan chains in said functional cores for diagnosis;

(g) issuing a STEP command for shifting in a predetermined number of clock cycles to a said functional core and running said system clock for said predetermined number of clock cycles in said functional cores;

(h) issuing a second SHIFT command or a second plurality of SHIFT_CHAIN commands for shifting data into and out of all said scan cells within said selected scan chains in said functional cores for diagnosis;

(i) repeating selected steps of (d)-(h) in any selected order at any time until functional diagnosis is done; and

(j) issuing a STOP command for generating a stop control signal to control said DFD circuitry in said functional cores.

67. The method of claim 66, further comprising providing a central DFD controller for accepting said commands and generating said functional debug mode and said control signals to control said DFD circuitry; wherein said DFD controller interfaces with said DFD circuitry and a TAP (test access port) controller in said integrated circuit; and wherein said TAP controller is constructed according to a selected Boundary-scan Standard.

68. The method of claim 66, wherein said selected fault type is used to detect or locate single or multiple errors arising from stuck-type faults or non-stuck-type delay faults in a said selected functional core; wherein

said stuck-type faults include stuck-at faults, bridging faults, and IDDQ (IDD quiescent current) faults; and wherein said non-stuck-type delay faults include transition (gate-delay) faults, path-delay faults, memory read/write faults, and multiple-cycle delay faults.

69. The method of claim 66, wherein said RESET command further comprises selectively using a third SHIFT command or a third plurality of SHIFT_CHAIN commands to initialize said functional cores to a predetermined state.

70. A method for testing, debugging, or diagnosing scan cores, memory BIST (built-in self-test) cores, logic BIST cores, and functional cores in an integrated circuit, each core having a selected fault type and each core type comprising a DFD (design-for-debug) circuitry; said method comprising:

(a) issuing a RUN_SCAN command for generating a scan test mode to control said DFD circuitry in said scan cores;

(b) issuing a RUN_MBIST command for generating a MBIST test mode to control said DFD circuitry in said memory BIST cores;

(c) issuing a RUN_LBIST command for generating a LBIST test mode to control said DFD circuitry in said logic BIST cores;

(d) issuing a DBG_SCAN command for generating a scan debug mode to control said DFD circuitry in said scan cores;

(e) issuing a DBG_MBIST command for generating a MBIST debug mode to control said DFD circuitry in said memory BIST cores;

(f) issuing a DBG_LBIST command for generating a LBIST debug mode to control said DFD circuitry in said logic BIST cores;

(g) issuing a DBG_FUNCTION command for generating a functional debug mode to control said DFD circuitry in said functional cores;

(h) issuing a SELECT command for shifting in selected cores and said selected fault types to be debugged or diagnosed to the DFD selector of said DFD circuitry in said scan cores, said memory BIST cores, said logic BIST cores, or said functional cores;

(i) issuing a SHIFT command for shifting data into and out of selected scan cells in said scan cores, said memory BIST cores, said logic BIST cores, or said functional cores;

(j) issuing a SHIFT_CHAIN command for shifting data into and out of all scan cells within selected scan chains in said scan cores, said logic BIST cores, or said functional cores;

(k) issuing a CAPTURE command for capturing results into all said scan cells in said scan cores or said memory BIST cores;

(l) issuing a SKIP command for generating a skip control signal to control said DFD circuitry in said memory BIST cores;

(m) issuing a RESET command for generating a reset control signal to control said DFD circuitry in said functional cores;

(n) issuing a BREAK command for generating a break control signal to control said DFD circuitry in said functional cores;

(o) issuing a RUN command for generating a run control signal to control said DFD circuitry in said memory BIST cores, said logic BIST cores, or said functional cores;

(p) issuing a STEP command for generating a step control signal to control said DFD circuitry in said functional cores;

(q) issuing a STOP command for generating a stop control signal to control said DFD circuitry in said scan cores, said memory BIST cores, said logic BIST cores, or said functional cores; and

(r) repeating selected steps of (a)-(q) in any predetermined order until testing, debugging, or diagnosis of said integrated circuit is done.

71. The method of claim 70, further comprising providing a central DFD controller for accepting said commands and generating said test modes, said debug modes, and said control signals to control said DFD circuitries; wherein said DFD controller interfaces with said DFD circuitries and a TAP (test access port) controller in said integrated circuit; and wherein said TAP controller is constructed according to a selected Boundary-scan Standard.

72. The method of claim 70, wherein said selected fault type is used to detect or locate single or multiple errors arising from stuck-type faults, non-stuck-type delay faults, or data retention faults in said selected core; wherein said stuck-type faults include stuck-at faults, bridging faults, and IDDQ (IDD quiescent current) faults; and wherein said non-stuck-type delay faults include transition (gate-delay) faults, path-delay faults, memory read/write faults, and multiple-cycle delay faults.

73. The method of claim 71, wherein said DFD controller or each said DFD circuitry is selectively placed inside or external to said integrated circuit.

74. The method of claim 70, wherein said commands are selectively combined with other JTAG instructions, including BYPASS, SAMPLE, EXTEST, HIGHZ, CLAMP, and

ID_CODE, to test, debug, or diagnose said integrated circuit.

75. The method of claim 70, wherein said commands are selectively used to test, debug, or diagnose physical failures in memory scan cores or other BIST cores generating error signals or cycle-end signals, including PLL (phase-locked loop) BIST cores, DAC (digital-to-analog) BIST cores, ADC (analog-to-digital) BIST cores, and ROM (read-only memory) BIST cores.

76. An apparatus for testing, debugging, or diagnosing scan cores, memory BIST (built-in self-test) cores, logic BIST cores, functional cores, memory scan cores, and other BIST cores generating error signals or cycle-end signals, including PLL (phase-locked loop) BIST cores, DAC (digital-to-analog) BIST cores, ADC (analog-to-digital) BIST cores, and ROM (read-only memory) BIST cores, in an integrated circuit; said apparatus comprising:

(a) means for inserting said DFD controller and said DFD circuitries in said integrated circuit;

(b) placing said integrated circuit on an evaluation board or system;

(c) using a low-cost DFT (design-for-test) debugger to issue said commands to said integrated circuit;

(d) using a fault diagnosis program on said low-cost DFT debugger to debug or diagnose physical failures in said integrated circuit; and

(e) using a graphical user interface on said low-cost DFT debugger to display the schematic and waveforms of selected signals, registers, or circuit connectivity in said integrated circuit.

77. The apparatus of claim 76, wherein said low-cost DFT debugger further comprises means for communicating with

said integrated circuit through a TAP (test access port) controller; wherein said TAP controller on said low-cost DFT debugger is connected to the TAP controller in said integrated circuit on said evaluation board or system.

78. The apparatus of claim 77, wherein said TAP controller on said low-cost DFT debugger is connected to the TAP controller in said integrated circuit further comprises means for connecting said TAP controller on said low-cost DFT debugger to said integrated circuit through other boundary-scan controlled integrated circuits on said evaluation board or system.

79. The apparatus of claim 76, wherein said fault diagnosis program and wherein said graphical user interface are selectively performed remotely through internet.

80. The apparatus of claim 76, wherein said low-cost DFT debugger further comprises an ATE (automatic test equipment).

81. A CAD (computer-aided design) method for synthesizing the DFD (design-for-debug) controller and a plurality of DFD circuitries in an integrated circuit to test, debug, or diagnose scan cores, memory BIST (built-in self-test) cores, logic BIST cores, functional cores, memory scan cores, and other BIST cores generating error signals or cycle-end signals, including PLL (phase-locked loop) BIST cores, DAC (digital-to-analog) BIST cores, ADC (analog-to-digital) BIST cores, and ROM (read-only memory) BIST cores; said CAD method comprising the computer-implemented steps of:

(a) compiling the HDL (hardware description language) code or netlist that represents said integrated circuit in physical form into a design database;

(b) performing DFD rule check for checking whether said design database contains any DFD rule violations;

(b) performing DFD rule repair until all said DFD rule violations have been fixed;

(c) synthesizing and stitching said DFD circuitries in selected said scan cores, said memory BIST cores, said logic BIST cores, and said functional cores;

(d) synthesizing and stitching said DFD controller for controlling said DFD circuitries;

(e) generating the synthesized DFD HDL code or netlist; and

(f) generating HDL test benches and ATE (automatic test equipment) test programs for verifying the correctness of said synthesized DFD HDL code or netlist in said integrated circuit.

82. The CAD method of claim 81, wherein said steps of (a)-(f) accept user-supplied DFD control information and report the results and errors if any.

83. The CAD method of claim 81, wherein said HDL test benches and ATE (automatic test equipment) test programs further comprise test programs for use on a low-cost DFT (design-for-test) debugger.